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# A Microcircuit 75-Counter

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## ABSTRACT

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A synchronous 75-counter using a repetitive, truncated, binary sequence is described. The counter is designed with the Veitch diagram simplification technique and is implemented with the Fairchild microcircuit J-K flip-flop. It is free from undesirable closed loops, returns to normal sequence in a maximum of one clock-pulse time, and is capable of speeds to 8 Mc at room temperature. Minimum and maximum power-supply voltage for correct sequencing is shown as a function of temperature from —50 to +125°C.


## I. INTRODUCTION

While investigating a possible system for bandwidth compression of digital television data, a requirement was found for a synchronous 75-counter. In addition, it was desirable to gain some familiarity with the high-speed, low-power microcircuitry recently made available. To satisfy both these objectives, the design of a synchronous 75-counter using the Fairchild J-K flip-flop and associated gates has been completed and tested.

The counter is to be used as a program control for a simple computer. Some of the output functions to be derived from the counter states are repetitive during each sequence of 75 clock pulses. To simplify the logical expressions for these functions, the first fifteen counter states are arranged to occur in a binary fashion. This sequence is then repeated five times to obtain the necessary 75 states.

## II. COUNTER STATES

The seven flip-flops used in the counter are labeled $A$ through $G$. Each state of the counter is tabulated in Table 1. The letter $m$ to the left identifies each state as a minterm in the usual manner, with the difference that $A$ is considered the least significant, and $G$ the most significant flip-flop position. By considering the flip-flop states thus, the plotting of the states in the Veitch diagram is somewhat simplified. For example, state 51 is represented by the binary number "1100110" with the most significant bit $G$ at the right. The locations of the minterms as defined above are shown in Fig. 1.

**Table 1. Counter sequence**

| m | State A | B | C | D | E | F | G | m | State A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 41 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 2 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 42 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 3 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 43 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 44 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 45 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 46 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 48 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 49 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 50 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 10 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 51 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 11 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 52 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 12 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 53 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 13 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 54 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 14 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 55 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 16 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 56 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 17 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 57 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 18 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 58 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 19 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 59 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 20 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 60 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 21 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 61 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 22 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 62 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 23 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 64 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 24 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 65 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 25 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 66 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 26 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 67 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 27 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 68 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 28 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 69 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 29 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 70 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 30 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 71 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 32 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 72 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 33 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 73 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 34 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 74 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 35 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 75 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 36 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 76 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 37 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 77 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 38 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 78 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 39 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 80 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

By plotting the minterms of Table 1 on the Veitch diagram, Fig. 2 is obtained. The minterms denoted by $X$ are the forbidden terms and do not normally occur during the counting sequence.

By plotting each minterm which causes flip-flop $A$ to be in a "one" condition at the next clock pulse, Fig. 3, the Veitch diagram equivalent of the application equation for flip-flop $A$, is obtained. A similar process results

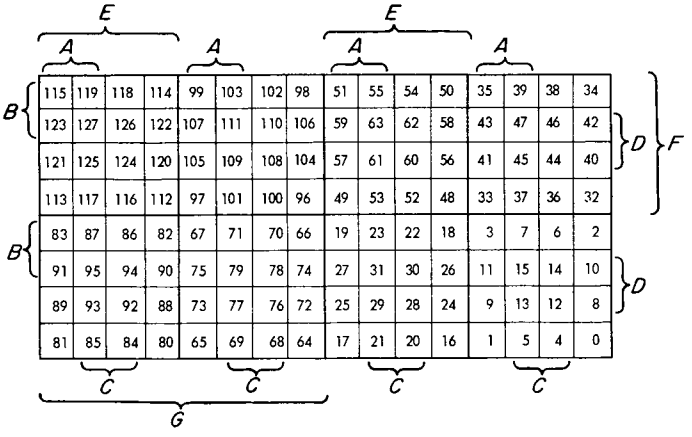


**Fig. 1. Veitch diagram of minterms**

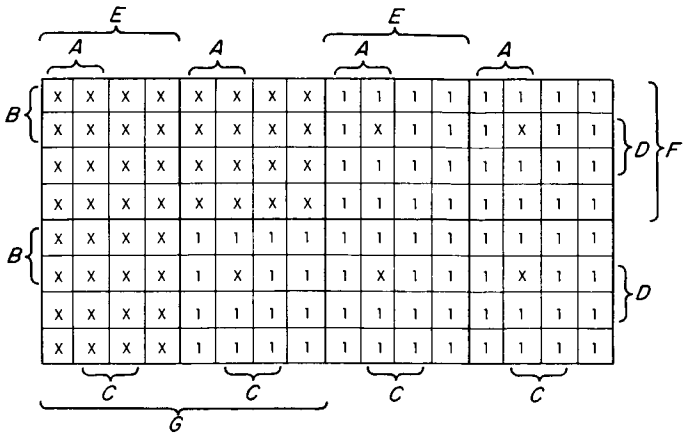


**Fig. 2. Counter states**

in diagrams for flip-flops $B$ through $G$. Following the rules for Veitch diagram simplification given in Ref. 1, p. 81, the input equations for J-K flip-flops may be derived from the application equations. The input equations are as follows:

$$J_A = \bar{B} + \bar{C} + \bar{D} \qquad K_D = BC$$

$$K_A = 1 \qquad J_E = BCD\bar{G}$$

$$J_B = A \qquad K_E = BCD\bar{G}$$

$$K_B = A + CD \qquad J_F = BCDE$$

$$J_C = AB \qquad K_F = BCDE$$

$$K_C = AB + BD \qquad J_G = BCDEF$$

$$J_D = ABC \qquad K_G = BCD$$

$A^{n+1} =$

| E | | | | E | | | |
|---|---|---|---|---|---|---|---|
| A | A | A | A | | | | |
| X X X X X X X X | 0 0 1 1 | 0 0 1 1 | | | | | |
| X X X X X X X X | 0 X 0 1 | 0 X 0 1 | } D | } F | | | |
| X X X X X X X X | 0 0 1 1 | 0 0 1 1 | | | | | |
| X X X X X X X X | 0 0 1 1 | 0 0 1 1 | | | | | |
| X X X X 0 0 1 1 | 0 0 1 1 | 0 0 1 1 | | | | | |
| X X X X 0 X 0 1 | 0 X 0 1 | 0 X 0 1 | } D | | | | |
| X X X X 0 0 1 1 | 0 0 1 1 | 0 0 1 1 | | | | | |
| X X X X 0 0 1 1 | 0 0 1 1 | 0 0 1 1 | | | | | |
| C | C | C | C | | | | |
| G | | | | | | | |

$E^{n+1} =$

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| X | X | X | X | X | X | X | X | 0 | X | 0 | 0 | 1 | X | 1 | 1 |
| X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | X | X | X | 0 | X | 0 | 0 | 1 | X | 1 | 1 | 1 | X | 1 | 1 |
| X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

$B^{n+1} =$

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| X | X | X | X | X | X | X | X | 0 | X | 0 | 1 | 0 | X | 0 | 1 |
| X | X | X | X | X | X | X | X | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| X | X | X | X | X | X | X | X | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| X | X | X | X | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| X | X | X | X | 0 | X | 0 | 1 | 0 | X | 0 | 1 | 0 | X | 0 | 1 |
| X | X | X | X | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| X | X | X | X | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

$F^{n+1} =$

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| X | X | X | X | X | X | X | X | 0 | X | 0 | 0 | 1 | X | 1 | 1 |
| X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| X | X | X | X | 0 | X | 0 | 0 | 1 | X | 1 | 1 | 0 | X | 0 | 0 |
| X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| X | X | X | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

$C^{n+1} =$

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| X | X | X | X | X | X | X | X | 1 | X | 0 | 0 | 1 | X | 0 | 0 |
| X | X | X | X | X | X | X | X | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| X | X | X | X | X | X | X | X | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| X | X | X | X | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| X | X | X | X | 1 | X | 0 | 0 | 1 | X | 0 | 0 | 1 | X | 0 | 0 |
| X | X | X | X | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| X | X | X | X | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

$G^{n+1} =$

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| X | X | X | X | X | X | X | X | 1 | X | 1 | 1 | 0 | X | 0 | 0 |
| X | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| X | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| X | X | X | X | 0 | X | 0 | 0 | 0 | X | 0 | 0 | 0 | X | 0 | 0 |
| X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

$D^{n+1} =$

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| X | X | X | X | X | X | X | X | 1 | X | 0 | 1 | 1 | X | 0 | 1 |
| X | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| X | X | X | X | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| X | X | X | X | 1 | X | 0 | 1 | 1 | X | 0 | 1 | 1 | X | 0 | 1 |
| X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Fig. 3. Application equations $A^{n+1}$, $B^{n+1}$, $C^{n+1}$, etc. through $G^{n+1}$**

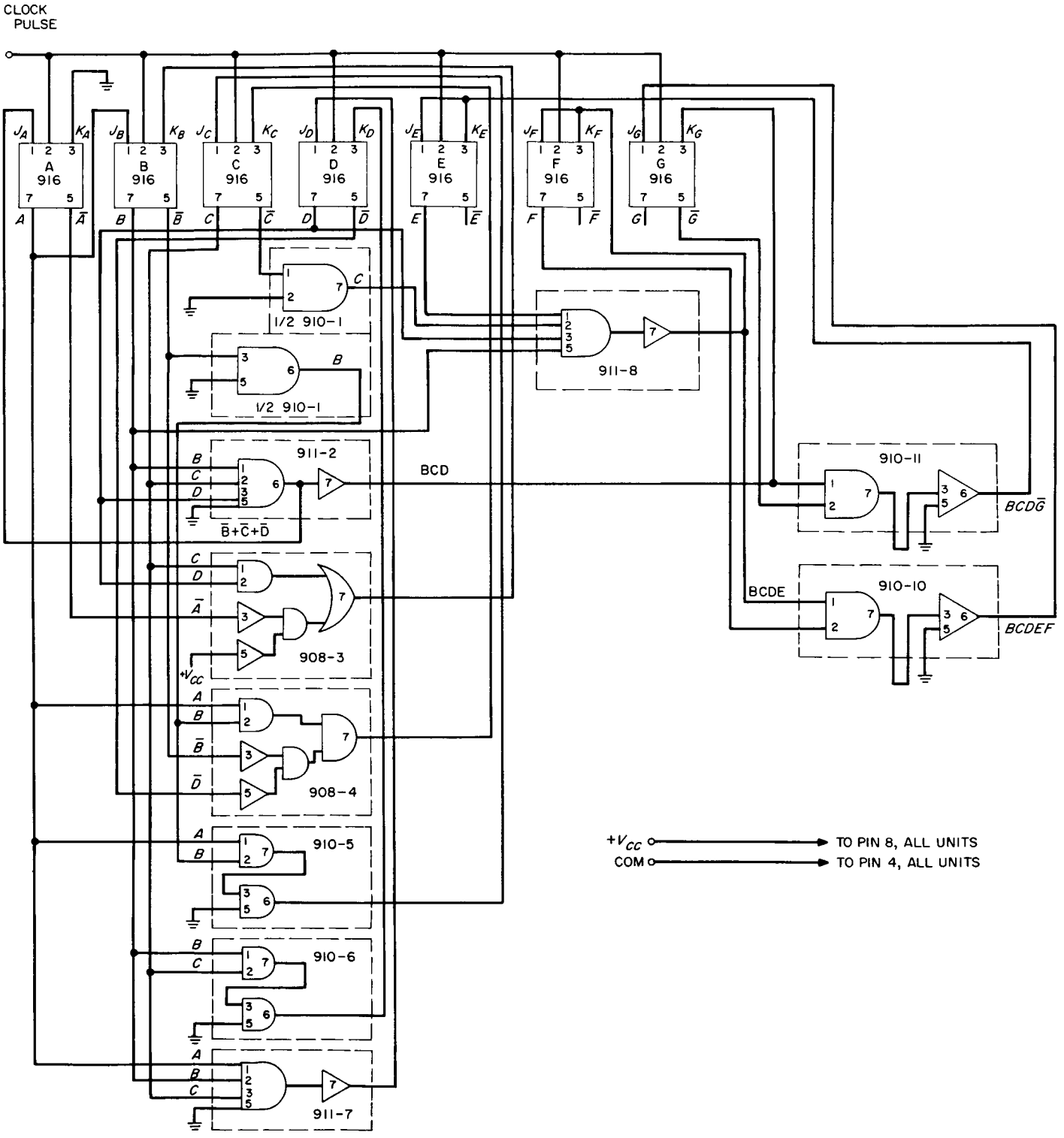


**Fig. 4. Logic schematic diagram**

These equations are implemented as shown in Fig. 4. The forbidden terms were examined for undesirable closed loops initiated by turn-on conditions or noise interference.

The method of interconnecting flip-flops *A*, *B*, *C* and *D* with *E*, *F* and *G*, greatly simplifies the examination of forbidden states. For example, should the counter arrive in the state identified by minterm 15, the input conditions for flip-flops *A*, *B*, *C* and *D* prior to the next clock pulse will be:

$$J_A = 0 \qquad J_B = 1 \qquad J_C = 1 \qquad J_D = 1$$

$$K_A = 1 \qquad K_B = 1 \qquad K_C = 1 \qquad K_D = 1$$

After the next clock pulse, *A*, *B*, *C* and *D* will be in state 0000, which is in the normal sequence. Similar examination of all forbidden states, some of which may be grouped into classes for simplification, indicates that the counter will always arrive in a normal counting state when starting from a forbidden state. In all cases this will occur in one clock pulse time.

## III. CONCLUSION

During testing of the breadboard counter, the maximum clock frequency for correct counting was found to be approximately 8 Mc. The failure to count properly above this frequency is a result of accumulated logical delay in the multilevel gates.

The longest accumulated delay occurs in the input logic for $J_G$ and amounts to the response of three cascaded gates, or approximately 0.2 $\mu$sec. This delay could be decreased by heavier loading of the flip-flop outputs and by different implementation of gate logic. With a decrease in logical delay, the counter could be made to operate at a higher clock frequency than is possible with the present configuration. Where auxiliary logical functions are to be generated from the counter, the present circuit has the advantage over one having shorter logical delays and higher loading at flip-flop outputs.

The circuit was tested over a temperature range of $-50$ to $+125$°C at a fixed clock rate of 10 kc. The operational envelope of the counter with Vcc variation and temperature is shown in Fig. 5. The upper limit of $+6$ v was imposed by system constraints and does not imply a failure of the counter above this voltage. Representative waveforms of the counter flip-flop outputs (at various temperatures) are shown in Fig. 6. The upper waveform is the output of the *D* flip-flop, the center waveform is the *G* flip-flop, and the lower waveform is the clock pulse.

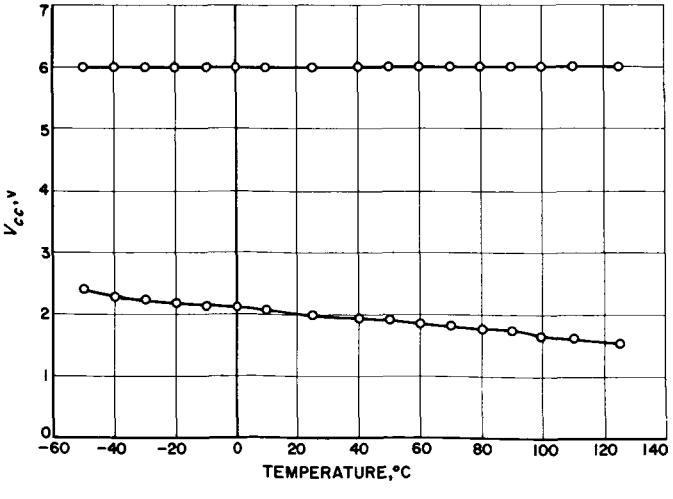


**Fig. 5. Operational envelope**

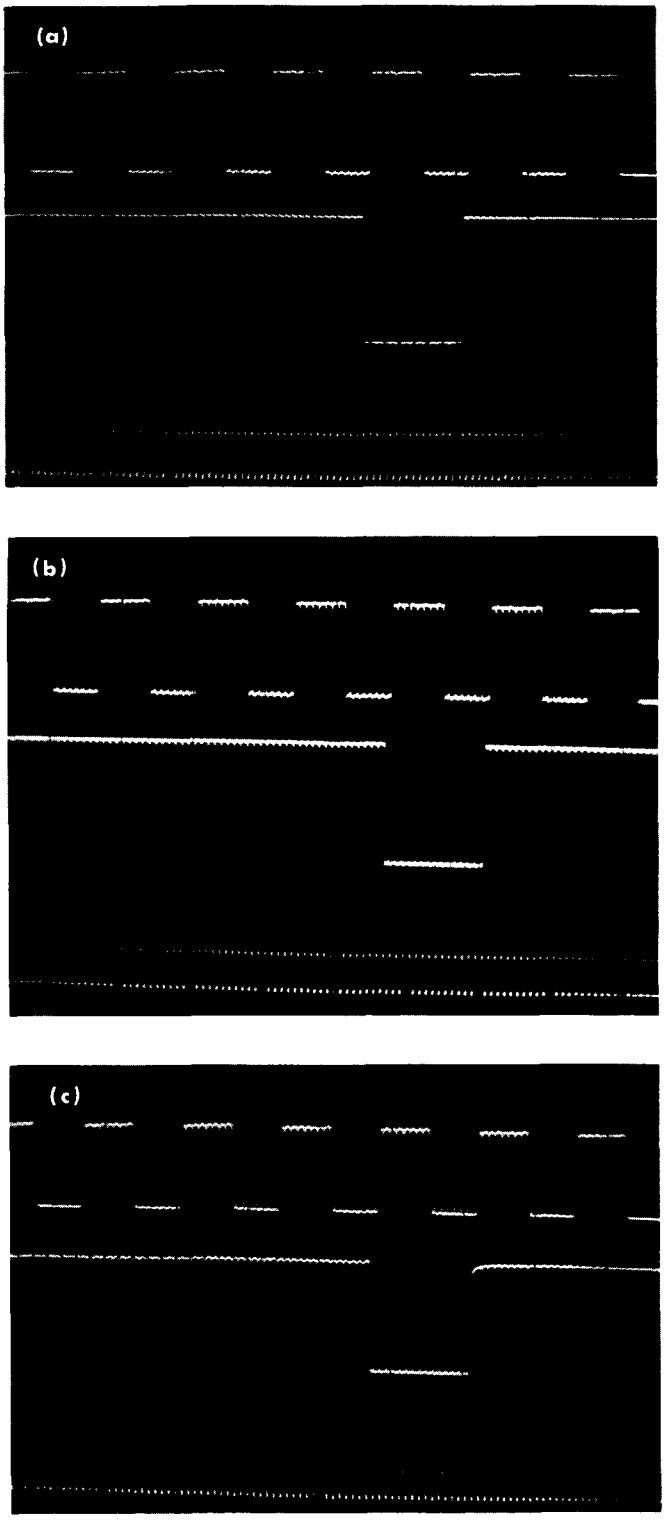


**Fig. 6. Representative waveforms of the counter flip-flop outputs at (a) −50°C, (b) +25°C, (c) +125°C**

Within the limitations of the equipment used for test and evaluation, the counter seemed quite insensitive to large variations of clock pulse amplitude and shape.

A practical difficulty experienced in construction of the breadboard was the intermittent connection made by the sockets. This problem was solved by rewiring the breadboard using Garlock type 69012-0528 sockets.

The power consumption of the counter at a supply voltage of 3v is approximately 0.4w.

## REFERENCE

1. Phister, M., *Logical Design of Digital Computers*, John Wiley & Sons, Inc., New York, 1958.